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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TESSERA 3.0-078 DIV	*Total Pages*	29
First Named Inventor or Application Identifier			
Express Mail Label No.	EM176988654US		

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 22] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [*Total Sheets* 5]
4. Oath or Declaration [*Total Pages* 2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* *[Note Box 5 below]*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: .....

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
    [ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08/739,303

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PATENT

TESSERA 3.0-078 DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of Joseph Fjelstad	:	
Divisional of Application No. 08/739,303 filed October 29, 1996	:	Group Art Unit:
Filed: Herewith	:	Examiner:
For: Semiconductor Chip Package With Fan-In Leads	:	Date: February 9, 1998
	X	

Assistant Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

After according a filing date to the above-identified Rule 53(b) Divisional Application, please amend the application as follows:

In the Claims

Cancel claims 12-20.

In the Title

Please amend the title of the application to --Method of Making a Semiconductor Chip Package--.

In the Specification

Page 1, before line 1, insert --This is a divisional of United States Patent Application Serial No. 08/739,303 filed October 29, 1996 the benefit of which is claimed under 35 U.S.C. § 120.--.

Abstract of the Disclosure

Please cancel the abstract presently on file and substitute therefore the following:

--Abstract of the Disclosure

EXPRESS MAIL LABEL NUMBER: EM176698854US

A method of making a compliant semiconductor chip package assembly includes providing a first dielectric protective layer on a contact bearing surface of a semiconductor chip wherein the semiconductor chip has a central region bounded by chip contacts of the semiconductor chip and wherein the dielectric protective layer has a plurality of apertures so that the chip contacts are exposed; providing a compliant layer atop the first dielectric protective layer within the central region wherein the compliant layer has a substantially flat top surface, a bottom surface that is attached to the first dielectric protective layer and sloping edges between the top surface and the bottom surface; and selectively electroplating bond ribbons atop the first dielectric protective layer in the compliant layer wherein each bond ribbon electrically connects each chip contact to a respective conductive terminal on the top surface of the compliant layer.--.

Remarks

The present application is a divisional of U. S. Patent Application Serial No. 08/739,303, filed October 29, 1996 and is in response to a restriction requirement of the Examiner in the '303 application. The present application is directed to the non-elected claims of the '303 application. The present Preliminary Amendment cancels claims 12-20 and amends the title and the abstract to more accurately describe the scope of the presently claimed invention.

The present Preliminary Amendment should be entered because it is fully supported by the specification and introduces no new matter.

For all of the reasons set forth above, prompt and favorable consideration of the amended application and allowance of claims 1-11 is respectively requested.

Respectfully submitted,

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Method of Making a

SEMICONDUCTOR CHIP PACKAGE ~~WITH FAN-IN LEADS~~

a1

Fig. A1

CROSS REFERENCE TO RELATED APPLICATIONS

The present application claims benefit of United States Provisional Application No. 60/007,128, filed October 31, 1995.

FIELD OF THE INVENTION

The present invention relates to semiconductor chip packaging. More particularly, the present invention relates to an improved compliant semiconductor package structure and methods for making the same.

BACKGROUND OF THE INVENTION

Complex microelectronic devices such as modern semiconductor chips require numerous connections to other electronic components. For example, a complex microprocessor chip may require many hundreds of connections to external devices.

Semiconductor chips commonly have been connected to electrical traces on mounting substrates by one of three methods: wire bonding, tape automated bonding, and flip-chip bonding. In wire bonding, the chip is positioned on a substrate with a bottom or back surface of the chip abutting the substrate and with the contact-bearing front or top surface of the chip facing upwardly, away from the substrate. Individual gold or aluminum wires are connected between the contacts on the chip and pads on the substrate. In tape automated bonding a flexible dielectric tape with a prefabricated array of leads thereon is positioned over the chip and substrate and the individual leads are bonded to the contacts on the chip and to pads on the substrate. In both wire bonding and conventional tape automated bonding, the pads on the substrate are arranged outside of the area covered by the chip, so that the wires or leads fan out from the chip to the surrounding pads. The area covered by the subassembly as a whole is considerably larger

than the area covered by the chip. This makes the entire assembly substantially larger than it otherwise would be. Because the speed with which a microelectronic assembly can operate is inversely related to its size, this presents a serious drawback. Moreover, the wire bonding and tape automated bonding approaches are generally most workable with chips having contacts disposed in rows extending along the periphery of the chip. They generally do not lend themselves to use with chips having contacts disposed in a so-called area array, i.e., a grid-like pattern covering all or a substantial portion of the chip front surface.

In the flip-chip mounting technique, the contact bearing surface of the chip faces towards the substrate. Each contact on the chip is joined by a solder bond to the corresponding pad on the substrate, as by positioning solder balls on the substrate or chip, juxtaposing the chip with the substrate in the front-face-down orientation and momentarily melting or reflowing the solder. The flip-chip technique yields a compact assembly, which occupies an area of the substrate no larger than the area of the chip itself. However, flip-chip assemblies suffer from significant problems with thermal stress. The solder bonds between the chip contacts and substrate are substantially rigid. Changes in the size of the chip and of the substrate due to thermal expansion and contraction in service create substantial stresses in these rigid bonds, which in turn can lead to fatigue failure of the bonds. Moreover, it is difficult to test the chip before attaching it to the substrate, and hence difficult to maintain the required outgoing quality level in the finished assembly, particularly where the assembly includes numerous chips.

Numerous attempts have been made to solve the foregoing problem. Useful solutions are disclosed in commonly assigned United States Patents 5,148,265 and 5,148,266. Preferred embodiments of the structures disclosed in these patents incorporate flexible, sheet-like structures referred to as "interposers" or "chip carriers". The preferred chip carriers have a plurality

of terminals disposed on a flexible, sheet-like top layer. In use, the interposer is disposed on the front or contact bearing surface of the chip with the terminals facing upwardly, away from the chip. The terminals are then connected to the contacts of the chip. Most preferably, this connection is made by bonding prefabricated leads on the interposer to the chip contacts, using a tool engaged with the lead. The completed assembly is then connected to a substrate, as by bonding the terminals of the chip carrier to the substrate. Because the leads and the dielectric layer of the chip carrier are flexible, the terminals on the chip carrier can move relative to the contacts on the chip without imposing significant stresses on the bonds between the leads and the chip, or on the bonds between the terminals and the substrate. Thus, the assembly can compensate for thermal effects. Moreover, the assembly most preferably includes a compliant layer disposed between the terminals on the chip carrier and the face of the chip itself as, for example, an elastomeric layer incorporated in the chip carrier and disposed between the dielectric layer of the chip carrier and the chip. Such a compliant structure permits displacement of the individual terminals independently towards the chip. This permits effective engagement between the subassembly and a test fixture. Thus, a test fixture incorporating numerous electrical contacts can be engaged with all of the terminals in the subassembly despite minor variations in the height of the terminals. The subassembly can be tested before it is bonded to a substrate so as to provide a tested, known, good part to the substrate assembly operation. This in turn provides very substantial economic and quality advantages.

Commonly owned United States Patent 5,455,390 describes a further improvement. Components according to preferred embodiments of the '390 patent use a flexible, dielectric top sheet having top and bottom surfaces. A plurality of terminals are mounted on the top sheet. A support layer is disposed underneath the top sheet, the support layer having a bottom surface

remote from the top sheet. A plurality of electrically conductive, elongated leads are connected to the terminals on the top sheet and extend generally side by side downwardly from the terminals through the support layer. Each lead has a lower end at the bottom surface of the support layer. The lower ends of the leads have conductive bonding materials as, for example, eutectic bonding metals. The support layer surrounds and supports the leads.

Components of this type can be connected to microelectronic elements such as semiconductor chips or wafers by juxtaposing the bottom surface of the support layer with the contact-bearing surface of the chip so as to bring the lower ends of the leads into engagement with the contacts on the chip, and then subjecting the assembly to elevated temperature and pressure conditions. All of the lower ends of the leads bond to the contacts on the chip substantially simultaneously. The bonded leads connect the terminals of the top sheet with the contacts on the chip. The support layer desirably is either formed from a relatively low-modulus, compliant material, or else is removed and replaced after the lead bonding step with such a compliant material. In the finished assembly, the terminals desirably are movable with respect to the chip to permit testing and to compensate for thermal effects. However, the components and methods of the '390 patent provide further advantages, including the ability to make all of the bonds to the chip or other component in a single lamination-like process step. The components and methods of the '390 application are especially advantageous when used with chips or other microelectronic elements having contacts disposed in an area array.

Despite the positive results of the aforementioned commonly owned inventions, still further improvements would be desirable.

SUMMARY OF THE INVENTION

The present invention contemplates a method of creating a compliant semiconductor chip package assembly and the semiconductor chip package assembly created therefrom.

In the fabrication process first, a first dielectric protective layer is provided on a contact bearing surface of a semiconductor chip. The semiconductor chip has a central region bounded by the chip contacts and a set of apertures. The apertures in the dielectric protective layer are provided such that the chip contacts are exposed. This first dielectric protective layer may actually be the silicon dioxide passivation layer of the semiconductor chip.

Second, a compliant layer, preferably consisting of silicone, flexibilized epoxy, a thermosetting polymer or polyimide is provided atop the first dielectric protective layer is provided within the central region. The compliant layer is formed such that it has a substantially flat top surface and edges that gradually slope down to the top surface of the first dielectric protective layer. The sloping edges of the compliant layer may be manufactured to have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer such that both the first transition region and the second transition region have a radius of curvature.

Finally, bond ribbons are selectively electroplated atop both the first dielectric protective layer and the compliant layer such that each bond ribbon electrically connects each chip contact to a respective terminal position on the compliant layer. The terminal positions are the conductive elements that connect the finished assembly to a separate substrate, e.g. a printed circuit board.

The method described above may further include the step of providing for a second dielectric protective layer atop the bond ribbons and the compliant layer after the bond ribbon electroplating step is performed. This optional second dielectric protective layer is fabricated with a set of apertures that expose the underlying terminal positions on the compliant layer.

Additionally, the method described above may further include the optional step of providing for an encapsulant layer above the bond ribbons. If this optional step is performed, it is performed after the step of selectively electroplating the bond ribbons. Like the first dielectric layer, the encapsulant layer is fabricated with a set of apertures so that the terminal positions are exposed. The encapsulant layer material consists preferably of either a curable liquid, such as silicone, a flexibilized epoxy or a gel. This optional step may also be performed just prior to the optional step of providing for a second dielectric protective layer.

The method above can be applied simultaneously to a multiplicity of undiced semiconductor chips on a wafer or an array of diced semiconductor chips arranged in an array to form a corresponding multiplicity of compliant semiconductor chip packages.

The present invention also claims the structure of a unique compliant semiconductor chip package having fan-in type leads. The compliant semiconductor chip package is comprised of (1) a semiconductor chip having a plurality of peripheral bonding pads on a face surface thereof and a central region bound by the peripheral bonding pads; (2) a first dielectric protective layer having a first surface, a second surface and apertures, wherein the first surface of the first dielectric layer is joined to the face surface of the semiconductor chip and the peripheral bonding pads are exposed through the apertures; (3) a compliant layer having a top surface and a bottom surface, wherein the bottom surface of the compliant layer is joined to the second surface of the first dielectric layer within the central region of the semiconductor chip package; and (4) a plurality of electrically conductive bond ribbons, each bond ribbon having a first end that electrically couples to a respective peripheral bonding pad of the semiconductor chip and a second end that joins to the top surface of the compliant layer to form a package terminal.

The package terminals of the completed package are configured in an array that has an area smaller than the area bound by the peripheral bonding pads on the face of the semiconductor chip. In other words, the package has fan-in leads that permits minimization of the overall package size.

For increased reliability, the compliant layer has sloped peripheral edges so that the overlying bond ribbons are curved rather than kinked.

The compliant semiconductor chip package may also have a compliant layer characterized by an array of bumped protrusions. The bumped protrusions support the overlying conductive terminal position ends of the bond ribbons and function as conductive balls that join to a substrate thus forming a ball grid array type interconnection. Alternate to the bumped protrusions, the compliant layer may have an array of concavities that are useful for placement of solder balls into each concavity. This arrangement is also useful for a ball grid array type interconnect.

The foregoing and other objects and advantages of the present invention will be better understood from the following Detailed Description of a Preferred Embodiment, taken together with the attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a cross-sectional view of a semiconductor chip assembly at the beginning of a fabrication process.

Figure 1B is a cross-sectional view of the semiconductor chip assembly after a first step of the fabrication process, showing a deposited or laminated dielectric passivation layer.

Figure 1C is a cross-sectional view of the semiconductor chip assembly after a second step of the fabrication process, showing a deposited or laminated compliant layer within the central region of the semiconductor chip contact-bearing surface.

Figure 1D is a cross-sectional view of the semiconductor chip assembly after a third step of the fabrication process, showing a conductive seed layer that has been sputtered over the assembly.

Figure 1E is a cross-sectional view of the semiconductor chip assembly after a fourth step of the fabrication process, illustrating how after a photolithographic step conductive bond ribbons can be formed over the assembly.

Figure 1F is a cross-sectional view of the semiconductor chip assembly after a fifth step of the fabrication process, showing how the assembly is coated with a second dielectric protective layer.

Figure 2 is a perspective view of the semiconductor chip assembly after the bond ribbons have been formed over the compliant layer but before the second dielectric protective layer is coated.

Figure 3 is a plan view of a wafer having a multiplicity of semiconductor chips, illustrating how said multiplicity of semiconductor chips can be simultaneously packaged using the semiconductor chip assembly process depicted in Figures 1A-1F.

Figure 4 is a cross-sectional view of an alternate embodiment of the present invention, illustrating the use of a low modulus encapsulant material to provide further support and stress relief to the bond ribbons.

Figure 5A is a cross-sectional view of an alternate embodiment of the present invention, illustrating the formation of bumped protrusions in the compliant layer that raise the overlying terminals such that the terminals form an array over the top surface of the compliant layer.

Figure 5B is a perspective view of the embodiment shown in Figure 5A.

Figure 6A is a cross-sectional view of an alternate embodiment of the present invention, illustrating the formation of concave areas in the compliant

layer such that the overlying terminals have cup-like depressions useful for accurate placement of solder balls.

Figure 6B is a perspective view of the embodiment shown in Figure 6A.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Figures 1A-F illustrate a side view of the process of creating the compliant chip package of the present invention on the face surface of a single die, on the face surfaces of multiple die arranged in a coplanar array or on the face surface of an undiced silicon wafer which may be subsequently diced into individual packaged chips or multi-chip modules.

Figure 1A shows a single semiconductor chip 100 with a contact bearing face surface 120. The contacts 110 on the face surface 120 are typically aligned in a peripheral region 112 and further define a central region 115 therein. In Figure 1B, a dielectric passivation layer is deposited or adhered onto the face surface 120 of the chip 100. The passivation layer may simply be the SiO_2 passivation layer (not shown) commonly found on the contact bearing surface of semiconductor chips, or a separate dielectric passivation layer 130 may be used, such as an epoxy resin, a polyimide resin, photo-imagable dielectric, etc. If the separate passivation layer 130 is used, the passivation layer 130 may be spun onto and built up to a planar sheet-like form on the face surface 120 or a dielectric sheet may be laminated to the face surface 120 using any of a number of electronic grade adhesives commonly known and used by those skilled in the art. The passivation layer 130 covers the face surface 120 of the chip 100 while leaving the chip contacts 110 exposed so that a bond ribbon may be plated thereon in a later step, as described below. Typically, this will be done by depositing or adhering the passivation layer 130 in a continuous sheet on the face surface 120 of the chip 100. A registering system, such as an automatic vision

system, is used to locate the contacts 110. If a photo-imagable dielectric is used, the passivation layer 130 may be exposed and developed without exposing the area above the contacts 110, that unexposed area may then be removed. Another removal process which can be used is to use a pulse of directed energy, such as an excimer laser, to selectively remove the passivation layer 130 above the contacts 110. Alternately, a continuous dielectric sheet already having set contact holes may be registered and laminated to the chip 100.

In the next step, as illustrated in Figure 1C, a compliant layer 140 is deposited or laminated onto the exposed surface of the passivation layer 130. The compliant layer 140 may be stenciled, screened or transfer molded onto the passivation layer 130 using a curable liquid which, when cured, adheres to the passivation layer 130. Alternately, the compliant layer 140 may be adhered to the exposed surface of the passivation layer 130 in the form of cured compliant pads using the aforementioned electronic grade adhesives. The compliant layer 140 has a substantially flat top surface 147 which further typically has a gradual, sloping transition 145 between the face surface 120 of the chip 100 and the top surface 147. This transition 145 may follow a line of curvature from the passivation layer 130 to a substantially flat top surface 147 or may simply be canted at an angle such that the transition 145 is not too vertically oriented in relation to the passivation layer 130 and the top surface 147. The compliant layer 140 itself may be formed from a wide variety of materials; however, preferably, a low modulus of elasticity material is used as the compliant layer 140. Compliant interposers typically are fabricated from polymeric and other materials such as silicones, flexibilized epoxy, polyimides and other thermosetting polymers, fluoropolymers and thermoplastic polymers. Also, the interposer may be a composite incorporating plural materials. The interposer may consist of, or incorporate, a foam or mesh layer. The flexibility of the interposer depends on the

thickness and configuration of the interposer, as well as on the properties of the materials used therein. Thus, a flexible interposer, capable of buckling or wrinkling to accommodate relative movement, can be fabricated from high elastic modulus materials, normally considered as "rigid" provided that these materials are present in thin layers. Relatively soft materials and foams can be used in greater thicknesses and still provide a highly flexible interposer. Moreover, such soft materials and foams provide a highly compliant interposer, i.e., an interposer which is readily compressible in the directions perpendicular its surfaces and which therefore permits movement of the terminals in these directions.

A plating seed layer 150 is then deposited atop the aforementioned assembly, as shown in Figure 1D, typically using a sputtering operation. Typical plating seed layer materials include palladium (for electroless plating), titanium, tungsten, nickel, chromium; however, primarily copper seed layers are used. Figure 1E shows the next step in which photoresist 160 is applied to the exposed top surfaces of the assembly and then exposed and developed such that bond ribbons 170 may be plated within defined areas to form conductive paths electrically connecting the chip contacts 110 near a first end region of the ribbons 170 to terminals 175 comprising the second end region of the ribbons 170. This is perhaps more easily seen in the perspective view shown in Figure 2. As shown, the ribbons 170 are plated directly onto the contacts 110 and extend in a "fan-in" arrangement from the peripheral region 112 to the central region 115 of the face surface 120 of the chip 100 atop the compliant layer 140. Possible bond ribbon materials include copper, gold, nickel, and alloys, combinations and composites thereof, among others. Since the bond ribbons 170 are plated directly onto the chip contact/compliant layer themselves, there is no need to develop a process for bonding the ribbons 170 to the contacts, as is necessary with most other approaches such as TAB, beam lead or wirebonding. This provides a

significant cost savings because specialized thermocompression or ultrasonic bonders and their bonding tools need not be purchased or maintained. It is important, however, that the material selected for the bond ribbon 170 be compatible with the chip contact 110 material, which is typically aluminum. Otherwise, a phenomenon called Kirkendahl Voiding (voids created at the boundary of two metals having different interdiffusion coefficients) may cause voiding along the boundary of the two metals (ribbon/contact) leading to intermetallic degradation and embrittlement of the bond ribbon 170 itself making the lead/bond susceptible to failure during thermal cycling. Alternately, one or more barrier metals may be plated atop the chip contacts 110 prior to the bond ribbon plating step to thereby ensure the compatibility of materials.

As shown in Figure 1F, preferably, a dielectric layer 180 is deposited or laminated over the top of the assembly so that only the terminals 175 are exposed. The dielectric layer may be comprised of a screened, exposed and developed or laminated sheet photo resist material or may be comprised of pyralene, epoxy resin, polyimide resin, fluoropolymer, etc. which is deposited or laminated on to the assembly, as described above in relation to the passivation layer 130. The terminals 175 may then be electrically connected to a circuitized substrate, such as a printed wiring board.

Typically, a solder ball or a solid-core solder ball will be used to create this electrical connection. The dielectric layer 180 is thus used as a solder mask to ensure that the solder does not electrically short between adjacent bond ribbons 170. Oxide layers and other surface contaminates typically build up on the surface of many types of metal (copper, nickel, etc.). Although not shown in Figure 1F, the terminals 175 are typically flash plated with a thin layer of gold (approximately 0.25 to 0.5 microns) to inhibit the formation of these oxide layers. The gold layer is kept very thin so that it does not appreciably affect the aforementioned solder joint by dissolving into

the solder to an amount which would embrittle the resulting solder joint between the terminal and a circuitized substrate.

The configuration of the above described chip package allows the package to mechanically decouple the chip 100 from an attached circuitized substrate (not shown). Typically, solder connections between the chip and the circuitized substrate are woefully inadequate to compensate for the thermal mismatch problem during temperature cycling of the chip. The combination of the compliant layer 140 and the flexible bond ribbons plated thereon allow the package to compensate for much of the TCE mismatch problem by giving limited movement of the terminals in the X, Y and Z directions with respect to the chip contacts 110 thereby minimizing the stress placed on the solder connections themselves, without imposing substantial forces on the bond between the ribbons 170 and the chip contacts 110. Further, because the compliant layer 140 is compressible, it also has the effect of compensating for any terminals 175 which are not perfectly planar with respect to its adjacent terminals when the terminals 175 are abutted against and coupled to the circuitized substrate. However, the top surface 147 of the compliant layer 140 should be made as flat and planar as possible so that the terminals 175 all lie in or near the same plane in order to minimize the amount of pressure needed to be placed on the bottom surface 125 of the chip 100 to ensure that all of the terminals/solder balls are electrically connected to a circuitized substrate.

As illustrated in Figure 3, the chip package described above in relation to Figures 1 and 2 may also be provided in the form of a multiplicity of packages on a wafer incorporating a plurality of individual, undiced chips, all of the same design or of differing designs. As shown, an array of individual passivation layers 230 may be deposited or laminated onto the face surface 220 of the wafer 200 leaving the chip contacts 210 of the various individual chips exposed, as described above. This arrangement is shown to better

define the individual chips within the wafer. Preferably, however, a single passivation layer 230 is deposited or laminated onto the face surface 220 leaving the contacts 210 exposed. Individual compliant layers 240, as described above, are deposited or laminated onto the central regions of each of the individual chips within the wafer 200. The steps found in Figure 1A-F are then performed, as described above, to create a plurality of connected individually packaged chips on the face surface 220 of the wafer 200. Each packaged chip having bond ribbons 270 which are connected at one end to contacts 210 and extending in to a central region of the respective chip in a fan-in fashion atop a respective compliant layer 240 and ending with a terminal 275 on the top surface 247 of the compliant layer 240. After the individual packages are completed, the individual chips may be separated from the wafer 200 and from one another, as by cutting the wafer 200 using conventional wafer severing or "dicing" equipment commonly utilized to sever wafers into individual chips. This procedure yields a plurality of packaged chip subassemblies, each of which may be secured to an individual circuitized substrate. Alternately, the chips may be separated from the wafer 200 in multi-chip arrangements of multiples of the same or different operational chips. The wafer level embodiment shown in Figure 3 could be simulated using a panel of individual chips spaced apart from one another in a processing boat. The face surfaces of the individual chips would be coplanar with respect to one another to simulate the face surface 220 of the wafer 200. The chips above described steps would be performed and the chips would be separated if desired.

In the alternate embodiment shown in Figure 4, a low modulus encapsulant material 290 may be deposited around the exposed surfaces of the bond ribbons 170' leads prior to the step shown in Figure 1F of depositing or laminating the assembly with the dielectric layer 180'. The encapsulant material 290 may have properties similar to those of rubber, gum or gel.

Typical encapsulation materials include curable liquid or cured pads comprised of silicone, flexibilized epoxy, gels, thermoplastics, etc. If the encapsulant 290 is applied as a curable liquid, a fixture may be made such that the liquid flows around the bond ribbons 170' but does not flow on top of the terminals 175' to ensure that solder balls may be subsequently electrically connected to the terminals 175', as described above. Alternately, a machine such as a Camalot 1818 manufactured by Camalot Systems, Inc. of Havermill, MA may be used to flow the liquid encapsulant into the desired areas. After the liquid is deposited, it may be cured by any number of ways depending on the encapsulant material 290 used, e.g. heat, infrared energy, etc. The encapsulant 290 gives each of the bond ribbons 170' more support and further spreads some of the stress away from the ribbons 170' thus allowing a larger TCE mismatch between the chip and a circuitized substrate, as described above. After curing of the encapsulant 290, the dielectric layer 180' may be deposited or laminated thereto.

In another alternate embodiment, a conductive material such as beryllium copper, or a super plastic or shape memory alloy (such as Nitinol), is sputtered or otherwise deposited across the entire exposed surface of the chip/passivation layer/compliant layer (100/130/140) combination, shown in Figure 1C. The conductive material may then be etched using industry standard photolithographic techniques resulting in a multiplicity of bond ribbons positioned and configured much like the bond ribbons 170 shown in Figure 1E and Figure 2. In this embodiment, as described above, a barrier metal, such as a flash plated layer of gold, may first be plated to the chip contacts to ensure compatibility of the electrical connection between the chip contact and the bond ribbon. Likewise, a flash plated layer of gold may be plated atop the exposed surface of the terminal. Also, the entire exposed surface of the bond ribbon could be plated with a thin layer of gold to

increase the overall conductivity of such super plastic leads. A dielectric layer is next deposited or laminated as shown in Figure 1F.

Figure 5A shows a side view and Figure 5B a perspective view of another embodiment, according to the present invention. In this embodiment, the compliant layer 140' has protrusions 300 on its top surface 147'. These protrusions 300 may be integral with the compliant layer 140' or may be deposited or laminated onto the top surface 147' subsequent to the formation of the compliant layer 140'. The protrusions 300 may be formed of compliant, elastomeric material, such as the material comprising the compliant layer 140', or may be comprised of a semi-rigid or rigid material. The bond ribbon terminals 175' are plated on top of the protrusions 300 thereby providing raised surfaces which may be connected to a circuitized substrate. This technique allows for connection to such a substrate using less solder and without the need to accurately position solid-core solder balls.

Figure 6A shows a side view and Figure 6B a perspective view of another embodiment, according to the present invention. In this embodiment, concave areas 310 are created in the compliant layer 140''. These concave areas 310 may be create in the formation of the compliant layer 140'' or may be created subsequent to the formation of the compliant layer 140''. The bond ribbon terminals 175'' are plated within the concave areas 310 creating conductive "cup-like" areas on the top surface 147'' of the compliant layer 140''. Solder or solid-core solder balls are then placed within these areas 310 and reflowed to attach the package to a circuitized substrate, as described earlier. This technique allows for the accurate placement of solder or solid-core solder balls by allowing them to be deposited and retained within the cup-like areas.

As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention as defined by the claims, the foregoing description of the preferred

embodiments should be taken by way of illustration rather than by way of limitation of the invention set forth in the claims.

WHAT IS CLAIMED IS:

1. A method of creating a compliant semiconductor chip package assembly comprising the steps of:

providing a first dielectric protective layer on a contact bearing surface of a semiconductor chip, wherein the semiconductor chip has a central region bounded by chip contacts of the semiconductor chip and wherein the dielectric protective layer has a plurality of apertures such that the chip contacts are exposed;

providing a compliant layer atop the first dielectric protective layer within the central region, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to the first dielectric protective layer and sloping edges between the top surface and the bottom surface; and

selectively electroplating bond ribbons atop the first dielectric protective layer and the compliant layer wherein each bond ribbon electrically connects each chip contact to a respective conductive terminal on the top surface of the compliant layer.

2. The method according to Claim 1 further including the step of providing a second dielectric protective layer atop exposed assembly elements on the terminal side of the assembly after the step of selectively electroplating the bond ribbons, wherein the second dielectric protective layer has a plurality of apertures such that the terminals are exposed.

3. The method according to Claim 1 wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

4. The method according to Claim 1 further including the step of providing for an encapsulant layer atop ~~the~~ exposed surface of the bond ribbons.

5. The method according to Claim 4 wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

6. The method according to Claim 4 further including the step of providing for a second dielectric protective layer atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures such that ~~the~~ terminal positions are exposed.

7. The method according to Claim 1 wherein a silicon dioxide passivation layer on the face surface of the semiconductor chip comprises the first dielectric protective layer.

8. The method according to Claim 1 further including the step of plating a barrier metal atop the semiconductor chip contacts, prior to the step of providing the compliant layer, whereby the barrier metal helps to prevent voiding at the boundary between the semiconductor chip contacts and the bond ribbons.

9. The method according to Claim 1 applied simultaneously to a multiplicity of undiced semiconductor chips on a wafer to form a corresponding multiplicity of compliant semiconductor chip packages, the method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

10. The method according to Claim 1 applied simultaneously to a multiplicity of adjacent semiconductor chips arranged in an array to form a corresponding multiplicity of compliant semiconductor chip packages, the method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

11. The method according to Claim 1 wherein the sloping edges of the compliant layer have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the

compliant layer and wherein both the first transition region and the second transition region have a radius of curvature.

12. A compliant semiconductor chip package assembly comprising:

a semiconductor chip having a plurality of peripheral chip contacts on a face surface thereof and a central region bound by the peripheral chip contacts;

a first dielectric protective layer having a first surface, a second surface and apertures, wherein the first surface of the first dielectric layer is attached to the face surface of the semiconductor chip and the apertures are aligned so that the chip contacts are exposed;

a compliant layer having a top surface, a bottom surface and sloping peripheral edges, wherein the bottom surface of the compliant layer is joined to the second surface of the first dielectric layer within the central region of the semiconductor chip package; and

a plurality of electrically conductive bond ribbons, each bond ribbon having a top surface, a bottom surface, a first end that electrically couples to a respective peripheral chip contact of the semiconductor chip, wherein each bond ribbon extends along the sloping edges to the top surface of the compliant layer and connects to a respective terminal.

13. The compliant semiconductor chip package of Claim 12 further including a second dielectric protective layer having a first surface that is attached to the exposed package assembly elements, wherein the second dielectric layer has a plurality of apertures such that the bonding pads of the semiconductor chip are exposed.

14. The compliant semiconductor chip package of Claim 12 further comprised of an encapsulant layer that is attached to the top surface of the bond ribbons.

15. The compliant semiconductor chip package of Claim 14 wherein the encapsulant layer material is selected from the group consisting of a curable liquid, silicone, flexibilized epoxy, thermoplastic and gel.

16. The compliant semiconductor chip package of Claim 12 wherein the plurality of package terminals are configured in an array having an area that is smaller than the area bound by the peripheral bonding pads on the face of the semiconductor chip.

17. The compliant semiconductor chip package of Claim 12, wherein the peripheral edge of the compliant layer has a first transition region near the top surface of the compliant layer and a second transition region near the second surface of the first dielectric protective layer and wherein the first and second transition regions have a radius of curvature.

18. The compliant semiconductor chip package of Claim 12, wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer and polyimide.

19. The compliant semiconductor chip package of Claim 12, wherein a plurality of bumped protrusions are provided and underly the plurality of package terminals such that an array of bumped package terminals is formed.

20. The compliant semiconductor chip package of Claim 12, wherein the top surface of the compliant layer has a plurality of concavities underlying the plurality of package terminals such that an array of concave-like package terminals is formed.

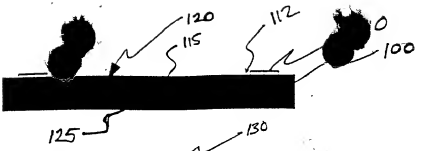

Figure 1A

Figure 1B

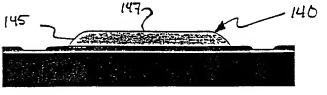

Figure 1C

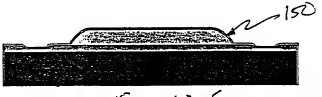

Figure 1D

Figure 1E

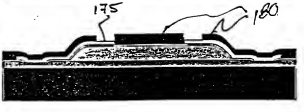

Figure 1F

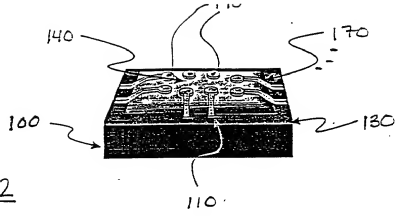

FIGURE 2

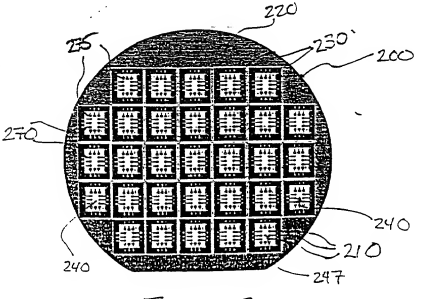

FIGURE 3

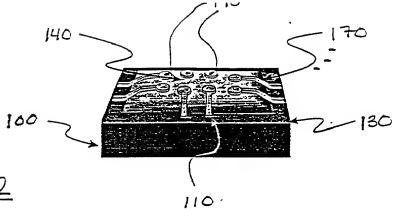

FIGURE 2

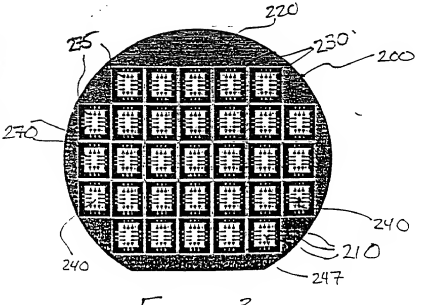

FIGURE 3

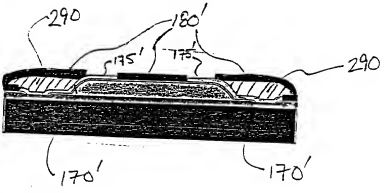

FIGURE 4

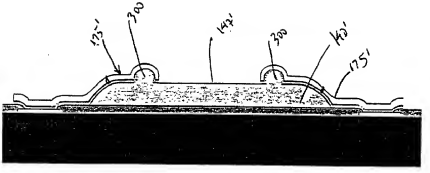

FIGURE 5A

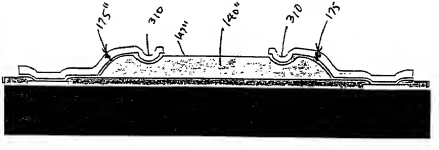

FIGURE 6A

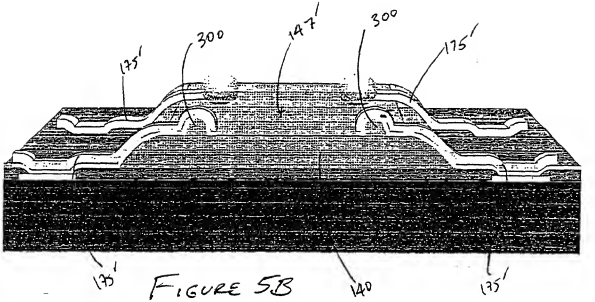

FIGURE 5B

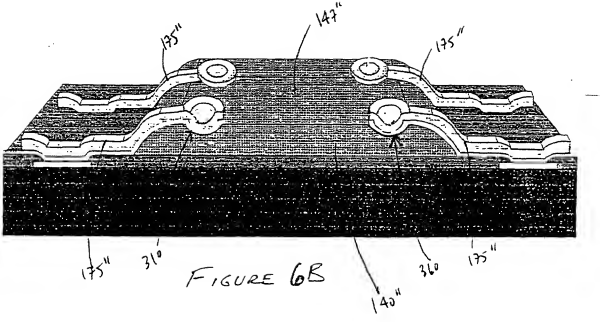

FIGURE 6B

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

ATTORNEY'S DOCKET NO.: TESSERA 3.0-078

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR CHIP PACKAGE WITH FAN-IN LEADS the specification of which

☐ is attached hereto

☒ was filed on October 29, 1996 as United States Application Number or PCT International Application Number 08/739,303 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (month, day, year)	PRIORITY CLAIMED
			YES ☐ NO ☐
			YES ☐ NO ☐
			YES ☐ NO ☐
LISTING OF FOREIGN APPLICATIONS CONTINUED ON PAGE 3 HEREOF ☐ YES ☒ NO			

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Application Number: 60/007,128 Filing Date: October 31, 1995

Application Number: Filing Date:

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Parent Application Serial Number: Parent Filing Date: Parent Patent No.:

U.S. Parent Application Serial Number: Parent Filing Date: Parent Patent No.:

PCT Parent Number: Parent Filing Date:

LISTING OF US APPLICATIONS CONTINUED ON PAGE 3 HEREOF: ☐ YES ☒ NO

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

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SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK 600 South Avenue West Westfield, New Jersey 07090	*(name and telephone number)* MARCUS J. MILLET (908) 654-5000 Fax: (908) 654-7866

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name): JOSEPH FJELSTAD

Inventor's signature _____ **Date** 5 MAR 97

Residence: Sunnyvale, CA Citizenship: U.S.A.
Post Office Address: 1168 Vasquez #1, Sunnyvale, CA 94086

Full name of second joint inventor, if any (given name, family name)

Second Inventor's signature _____ **Date** _____

Residence: Citizenship:
Post Office Address:

Full name of third joint inventor, if any (given name, family name):

Third Inventor's signature _____ **Date** _____

Residence: Citizenship:
Post Office Address:

Full name of fourth joint inventor, if any (given name, family name):

Fourth Inventor's signature _____ **Date** _____

Residence: Citizenship:
Post Office Address:

Full name of fifth joint inventor (given name, family name):

Fifth Inventor's signature _____ **Date** _____

Residence: Citizenship:
Post Office Address:

Full name of sixth joint inventor, if any (given name, family name):

Sixth Inventor's signature _____ **Date** _____

Residence: Citizenship:
Post Office Address:

Full name of seventh joint inventor, if any (given name, family name):

Seventh Inventor's signature _____ **Date** _____

Residence: Citizenship:
Post Office Address:

Full name of eighth joint inventor, if any (given name, family name):

Eighth Inventor's signature _____ **Date** _____

Residence: Citizenship:
Post Office Address:

☐ Additional inventors are being named on separately numbered sheets attached hereto.